

**Publication number:** JP2000285591

**Publication date:** 2000-10-13

**Inventor:** NISHINAGA KOICHI; MORITA KOJI; YAMASHITA TOSHIRO

**Applicant:** KOBE STEEL LTD

**Classification:**

- **International:** *G11B20/10; G10K15/02; G10L19/00; H04M11/08; G11B20/10; G10K15/02; G10L19/00; H04M11/08; (IPC1-7): G11B20/10; G10L19/00; H04M11/08*

- **European:**

**Application number:** JP19990087063 19990329

**Priority number(s):** JP19990087063 19990329

## Abstract of JP2000285591

Figure 1 is a block diagram of a system architecture. The diagram is divided into three main sections: a top section (10), a middle section (20), and a bottom section (30). The top section (10) contains a 'CPU' (11), a 'Memory' (12), and an 'Input Unit' (13). The middle section (20) contains a 'CPU' (21), a 'Memory' (22), and an 'Input Unit' (23). The bottom section (30) contains a 'CPU' (31), a 'Memory' (32), and an 'Input Unit' (33). The sections are interconnected via a bus system (14, 24, 34).

9/11/06